[the timing signals have peaks and zero crossings and wherein the predetermined characteristics in the timing signals constitute the peaks and zero crossings of the timing signals and wherein]

the timing signals have peaks and zero crossings that constitute the predetermined characteristics and wherein

the digitally processed signals have peaks and zero crossings and wherein the predetermined characteristics in the digitally processed signals constitute the peaks and zero crossings of the digitally processed signals.

106. (Amended) A method as set forth in claim 104 wherein the received signals are provided in packets and wherein

[the received signals in each packet include timing signals in a preamble and data signals following the preamble and wherein]

the phases of the digitally processed timing signals in each packet are adjusted

the digitally processed signals receiving in each packet the adjustments in the phases constitute the timing signals in the preamble in the packet.

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108. (Amended) A method as set forth in claim 106 wherein

[the digitally processed signals receiving in each packet the adjustments in the phases of the digitally processed signals also constitute the data signals in the packet.]

the phases of the digitally processed data signals in each packet are adjusted.

Claim 111, line 22, after "selecting" insert -- predicted --.

Claim 113, line 6, after "selecting" insert -- predicted --.

Claim 115, line 29, after "selecting" insert -- predicted --.

Claim 117, line 29, after "selecting" insert -- predicted --.

130. (Amended) A bidirectional data communication system comprising:

communication signals having individual ones of a plurality of analog levels to represent information;

a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line transmitting or receiving said communication signals;

a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line pairs;

a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including;

an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal; and

a <u>fully</u> digital <u>adaptive</u> equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels.

131. (Amended) A bidirectional data communication system according to claim [127] <u>130</u>, the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital converter operatively

responsive to said timing information and performing digital conversions at a rate defined thereby.

132. (Amended) A bidirectional data communication system according to claim [128] 131, wherein the communication signals are provided in packets, each packet comprising a preamble portion and a data containing portion, the preamble portion including timing signals.

133. (Amended) A bidirectional data communication system according to claim [129] 132, wherein the timing recovery circuitry comprises a first timing loop having a high gain stage and a second timing loop having a low gain stage, the first timing loop locking the analog to digital converter in phase with the preamble portion the second timing loop locking the analog to digital converter in phase with the data containing portion.

134. (Amended) A bidirectional data communication system according to claim [130] 133, wherein the first timing loop includes a high gain error generator, a loop filter, and an oscillator circuit, the high gain error generator responsive to characteristic values of the timing signals, and wherein the second timing loop includes a low gain error generator, a loop filter, and an oscillator circuit, the high gain error generator responsive to characteristic values of the data signals.

135. (Amended) A bidirectional data communication system according to claim 131, the digital adaptive equalizer further comprising;

a feed forward equalizer having an input receiving the digital signal from the analog to digital converter and an output;

a slicer coupled to receive the digital signal from the feed forward equalizer and outputting a signal <u>representing a symbol, the signal</u> characterized by the digital levels;

an adder disposed between the feed forward equalizer and the slicer; and

a decision feedback equalizer having an input receiving the signal output by the slicer and an output coupled to the adder, the adder summing the output of the decision feedback equalizer with the output of the feed forward equalizer.

136. (Amended) A bidirectional data communication system according to claim 132, wherein the plurality of signal lines comprises four unshielded twisted pairs defining a local area network.

137. (Amended) A bidirectional data communication system according to claim [133] <u>136</u>, wherein the local area network is an Ethernet network, the four unshielded twisted pairs comprising a first pair adapted for transmission, second and third pairs adapted for bidirectional transmission and reception, and a fourth pair adapted for reception.

138. (Amended) A bidirectional data communication system according to claim [134] <u>132</u>, wherein the communication signals are encoded to one of three analog levels, thereby representing information.

139. (Amended) A bidirectional data communication system according to claim [135] 137, wherein the transmitter block comprises three transmitters, the transmitters coupled respectively to the first, second and third unshielded twisted wire pairs, and wherein the receiver block comprises three receivers, the receivers coupled respectively to the second, third and fourth unshielded twisted wire pairs.

140. (Amended) A bidirectional data communication system comprising:

communication signals having individual ones of a plurality of analog levels to represent information;

a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line transmitting or receiving said communication signals;

a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line pairs;

a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including;

an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal;

an automatic gain control circuit coupled in feedback fashion to the analog to digital converter and operatively responsive to output signals therefrom to control the gain of received communication signals; and

a fully digital adaptive equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels.

141. (Amended) A bidirectional data communication system according to claim [137] 140, the digital adaptive equalizer further comprising;

a feed forward equalizer having an input receiving the digital signal from the analog to digital converter and an output;

a slicer coupled to receive the digital signal from the feed forward equalizer and outputting a signal representing a symbol, the signal characterized by the digital levels;

an adder disposed between the feed forward equalizer and the slicer; and

a decision feedback equalizer having an input receiving the signal output by the slicer and an output coupled to the adder, the adder summing the output of the decision feedback equalizer with the output of the feed forward equalizer.

142. (Amended) A bidirectional data communication system according to claim [138] 141, the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital converter operatively responsive to said timing information and performing digital conversions at a rate defined thereby.

143. (Amended) A bidirectional data communication system according to claim [139] 142, wherein the timing recovery circuitry comprises a first timing loop having a high gain stage and a second

timing loop having a low gain stage, the first timing loop locking the analog to digital converter in phase with the preamble portion the second timing loop locking the analog to digital converter in phase with the data containing portion.

144. (Amended) A bidirectional data communication system according to claim [140] 143, wherein the first timing loop includes a high gain error generator, a loop filter, and an oscillator circuit, the high gain error generator responsive to characteristic values of the timing signals, and wherein the second timing loop includes a low gain error generator, a loop filter, and an oscillator circuit, the high gain error generator responsive to characteristic values of the data signals.

REMARKS

Claims 1-144 are in the application with claims 105, 106, 108, 111, 113, 115, 117 and 130-144 having been amended. Of the claims under consideration, claims 1, 7, 14, 22, 28, 34, 41, 45, 52, 58, 64, 68, 72, 76, 81, 85, 93, 99, 104, 111, 115, 117, 119, 123, 129, 130,and 140 are the independent claims. Reconsideration and further examination are respectfully requested.

Initially, the reissue oath/declaration filed with the application was deemed defective because the declaration does not state whether the inventor is a sole inventor or a joint inventor of the invention claimed. In addition, the deceptive intent error statement was deemed defective because it only refers to those errors specified in the reissue oath/declaration.

In response, Applicants submit herewith an amended reissue oath/declaration that addresses the defects noted by the Examiner. Specifically, the inventors are identified as the "original, first